Claims Listing:

What is claimed is:

1. (previously amended) A method for designing an integrated circuit comprising:

partitioning a design into a plurality of function blocks;

designing a first one of said plurality of function blocks employing Verilog to produce a first block design;

designing a second one of said plurality of function blocks employing SPICE to produce a second block design;

converting said first block design from Verilog to SPICE to produce a converted first block design comprising a file including a subcircuit name identified by ".SUBCKT" heading, at least one node name, at least one discrete circuit element description, at least one output signal name, and a ".ENDS" statement;

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simulating operation of said converted first block design and said second block design; and

translating said converted first block design from SPICE to Verilog to produce a translated first block design.

2. (original) The method of claim 1 further comprising:

comparing said translated first block design with said first block design.

3. (previously amended) The method of claim 1 wherein said step of translating further comprises:

changing said ".SUBCKT" heading in said converted first block design to "module".

4. (previously amended) The method of claim 1 wherein said step of translating further comprises:

changing said ".ENDS" statement in said converted first block design netlist to "endmodule".

5. (previously amended) The method of claim 1 wherein said step of translating further comprises:

deleting said at least one discrete circuit element description in said converted first block design.

6. (previously amended) The method of claim 1 wherein said step of translating further comprises:

defining a wire name corresponding to said at least one node name in said converted first block design.

7. (previously amended) The method of claim 1 wherein said step of translating further comprises:

identifying said at least one output signal name in said converted first block design and defining a Verilog output signal using said output signal name.

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8. (previously amended) The method of claim 1 wherein said step of translating further comprises:

identifying said subcircuit name.

9. (previously amended) The method of claim 8 wherein said step of translating further comprises:

employing said subcircuit name as a module name.

10. (previously amended) A method for translating a SPICE netlist to Verilog comprising:

opening a SPICE file comprising a subcircuit name identified by a ".SUBCKT" heading, at least one input signal name, at least one circuit element, at least one discrete circuit element description, an output signal name, and a .ENDS statement;

translating said ".SUBCKT" heading in said SPICE file to "module";

translating said ".ENDS" statement in said SPICE file to "endmodule";

translating said at least one circuit element in said SPICE file to Verilog format; and

removing said at least one discrete circuit element description.

11. (original) The method of claim 10 further comprising:

saving the file.

12. (previously amended) The method of claim 10 wherein said step of translating further comprises:

identifying said input signal name in said SPICE file and defining a Verilog wire employing said input signal name.

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13. (previously amended) The method of claim 12 wherein said step of identifying further comprises:

identifying said input signal name through a naming convention.

14. (previously amended) The method of claim 12 wherein said step of identifying further comprises:

identifying said input signal name through a predefined delimiter.

15. (previously amended) The method of claim 10 further comprising:

identifying said subcircuit name in said SPICE file.

16. (previously amended) The method of claim 15 wherein said step of translating further comprises:

employing said subcircuit name as a Verilog module name.

17. (previously amended) An integrated circuit produced by the steps of:

partitioning a design into a plurality of function blocks;

designing a first one of said plurality of function blocks employing Verilog to produce a first block design;

designing a second one of said plurality of function blocks employing SPICE to produce a second block design;

converting said first block design from Verilog to SPICE to produce a converted first block design comprising a file including a subcircuit name identified by a ".SUBCKT" heading, at least one node name, at least one discrete circuit element description, at least one output signal name, and a ".ENDS" statement;

simulating operation of said converted first block design and said second block design; and

translating said converted first block design to Verilog to produce a translated first block design.

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18. (original) The integrated circuit of claim 17 further comprising:

comparing said translated first block design with said first block design.

19. (previously amended) The integrated circuit of claim 17 wherein said step of translating further comprises:

changing said ".SUBCKT" heading in said converted first block design to "module".

20. (previously amended) The integrated circuit of claim 17 wherein said step of translating further comprises:

changing said ".ENDS" statement in said converted first block design to "endmodule".

21. (previously amended) The integrated circuit of claim 17 wherein said step of translating further comprises:

deleting said discrete circuit element description in said converted first block design.

22. (previously amended) The integrated circuit of claim 17 wherein said step of translating further comprises:

defining a Verilog wire name corresponding to said at least one node name in said converted first block design.

23. (previously amended) The integrated circuit of claim 17 wherein said step of translating further comprises:

identifying said at least one output signal name in said converted first block design and defining a Verilog output signal using said output signal name.

24. (previously amended) The integrated circuit of claim 17 wherein said step of translating further comprises:

identifying said subcircuit name.

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25. (previously amended) The integrated circuit of claim 24 wherein said step of translating further comprises:

employing said subcircuit name as a module name.

26. (new) A method for designing an integrated circuit comprising:

partitioning a design into a plurality of function blocks;

designing a first one of said plurality of function blocks employing Verilog to produce a first block design;

designing a second one of said plurality of function blocks employing SPICE to produce a second block design comprising a file including at least one input signal name, at least one circuit element, at least one discrete circuit element description, an output signal name, and a .ENDS statement;

converting said second block design from SPICE to Verilog including translating said at least one circuit element in said file to Verilog format to produce a converted block design; and

simulating operation of said first block design and said converted block design using Verilog.

27. (new) An integrated circuit produced by the steps of:

partitioning a design into a plurality of function blocks;

designing a first one of said plurality of function blocks employing Verilog to produce a first block design;

designing a second one of said plurality of function blocks employing SPICE to produce a second block design comprising a file including at least one input signal name, at least one circuit element, at least one discrete circuit element description, an output signal name, and a .ENDS statement;

converting said second block design from SPICE to Verilog including translating said at least one circuit element in said file to Verilog format to produce a converted block design; and

simulating operation of said first block design and said converted block design using Verilog.